

Thickness-dependent charge transport in few-layer MoS₂ field-effect transistors

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Abstract

Molybdenum disulfide (MoS₂) is currently under intensive study because of its exceptional optical and electrical properties in few-layer form. However, how charge transport mechanisms vary with the number of layers in MoS₂ flakes remains unclear. Here, exfoliated flakes of MoS₂ with various thicknesses were successfully fabricated into field-effect transistors (FETs) to measure the thickness and temperature dependences of electrical mobility. For these MoS₂ FETs, measurements at both 295 K and 77 K revealed the maximum mobility for layer thicknesses between 5 layers (~3.6 nm) and 10 layers (~7 nm), with ~70 cm² V⁻¹ s⁻¹ measured for 5 layer devices at 295 K. Temperature-dependent mobility measurements revealed that the mobility rises with increasing temperature to a maximum. This maximum occurs at increasing temperature with increasing layer thickness, possibly due to strong Coulomb scattering from charge impurities or weakened electron–phonon interactions for thicker devices. Temperature-dependent conductivity measurements for different gate voltages revealed a metal-to-insulator transition for devices thinner than 10 layers, which may enable new memory and switching applications. This study advances the understanding of fundamental charge transport mechanisms in few-layer MoS₂, and indicates the promise of few-layer transition metal dichalcogenides as candidates for potential optoelectronic applications.

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(Some figures may appear in colour only in the online journal)

1. Introduction

Two-dimensional (2D) layered transition metal dichalcogenides (TMDs) have attracted intense attention as candidates to replace conventional Si technology [1–3]. Recent studies have demonstrated the potential of 2D layered materials for applications, such as field-effect transistors (FETs) [4–8], highly flexible transistors [9], and optoelectronics [10, 11]. Molybdenum disulfide (MoS₂), for example, has exhibited many unique optoelectronics properties, such as strong room temperature photoluminescence [12]. MoS₂ is covalently bonded in plane, allowing it to withstand high mechanical strain laterally, while weak Van der Waals interactions between layers lead to easy mechanical cleavage for tailoring

layer number or aiding transfer during exfoliation techniques. MoS₂ has an indirect bandgap of ~1.3 eV in the bulk and a direct bandgap of ~1.8 eV as the material approaches a monolayer [13], making devices produced from thin layers of MoS₂ fundamentally different from their bulk counterparts in terms of their electrical and optical properties. MoS₂-based devices have recently been demonstrated, including FETs [7, 14–16], photo-transistors [12], low power electronics [17, 18] and gate-tuned superconductors [19]. Also MoS₂ exhibits a lack of inversion symmetry and a valley-split valence band, leading to a valley Hall effect that is promising for valley- or spin-tronic devices [20, 21]. Despite these advances in the field, the mobility of FETs based on mono- or few-layer MoS₂ is still relatively low compared to that found

in the bulk. To address this shortcoming, many different approaches have recently been explored to enhance the mobility of 2D MoS₂ crystals, including the incorporation of high dielectric materials such as HfO₂ or Al₂O₃, or doping via the addition of a polymer electrolyte or ionic liquid on the top of the device [22–31]. However, despite these novel approaches few studies have addressed the crucial questions of the temperature dependent transport mechanisms and the optimal layer thickness for maximum mobility in 2D MoS₂ crystals.

Previous studies have presented the transport mechanisms of MoS₂ FET devices as corresponding to phonon-limited scattering at higher temperatures [7, 22], and variable range hopping (VRH) due to sulfur vacancies at lower temperatures [32]. The temperature dependence of mobility has been observed in either monolayer or few-layer MoS₂ crystals in previous reports [22, 25], however a systematic study of transport mechanisms versus layer thickness with temperature dependence has not yet been performed. It is essential to understand the underlying charge transport mechanisms for 2D MoS₂ with different number of layers (NLs) in order to assess the applicability of MoS₂ crystals for different potential electronic and optical applications.

In this study, mono- and few-layer MoS₂ crystals were exfoliated and transferred to SiO₂/Si substrates using a conventional adhesive tape method, and MoS₂ FET devices were fabricated to measure thickness and temperature dependences of electrical mobility. A maximum mobility of $\sim 70 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was observed at room temperature for 5L ($\sim 3.6 \text{ nm}$) flakes, however non-monotonic trends observed in the correlation between mobility and thickness both at room temperature and 77 K in the MoS₂ FET devices indicated that crystal layers with thicknesses between 5L ($\sim 3.6 \text{ nm}$) and 10L ($\sim 7 \text{ nm}$) were optimal for practical applications. The correlation of increasing temperature of peak mobility with increasing thickness is attributed to either the strong effect of Coulomb scattering or weakened in-plane electron–phonon interaction with increasing thickness. A metal–insulator transition (MIT) was observed for all thickness below 10L in our MoS₂ FET devices, with the limiting thickness of this phenomenon possibly related to the formation of a 2D electron gas with high carrier densities in MoS₂.

2. Experimental methods

The MoS₂ flakes were exfoliated from a bulk crystal onto a SiO₂/Si wafer using adhesive tape. An optical microscope (Nikon LV150) was used to identify the location and estimated thickness of several flakes by noting their contrast. A Bruker Dimension Icon atomic force microscope (AFM) was then used to refine the thickness estimates. Raman spectroscopy (Renishaw Raman Spectrometer, 532 nm excitation source and 50X objective) was used to verify the characteristic peaks of the MoS₂ samples. The FETs were fabricated on a single wafer using electron beam lithography (JEOL 9300), simultaneously exposing all of the devices to the same processing step to ensure uniformity. Using electron

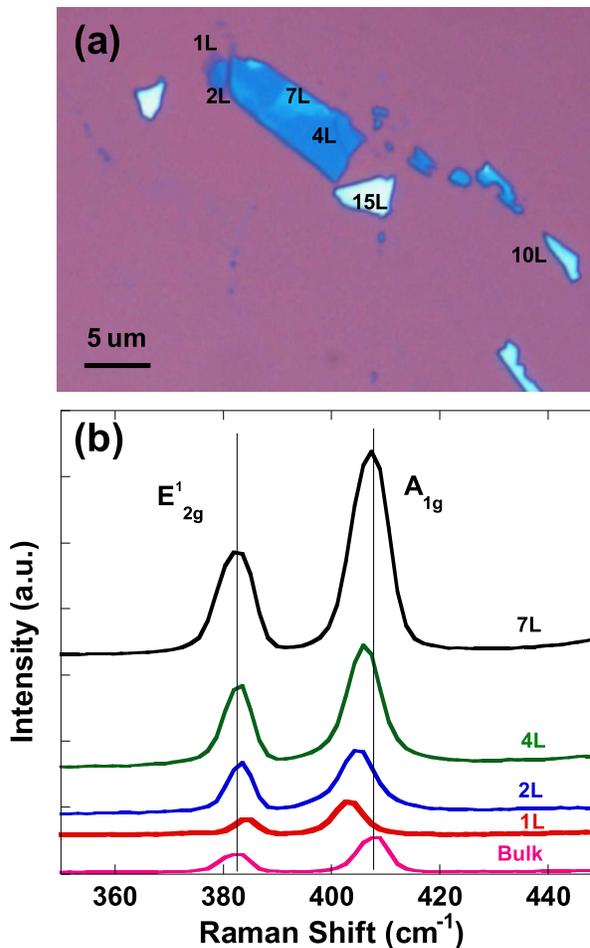


Figure 1. Optical microscope (OM) image and Raman spectrum of MoS₂ flakes using 532 nm excitation. (a) The OM image shows exfoliated MoS₂ flakes with various thicknesses as verified by AFM. Layer numbers are shown. (b) The Raman spectra show a shift of the characteristic peaks associated with in-plane (E'_{2g}) and out-of-plane (A_{1g}) vibrations as thickness is reduced. A bulk spectrum is shown for reference.

beam evaporation, layers of 5 nm thick Ti and 30 nm thick Au were then deposited to form source/drain electrodes. Finally, the electrical properties of the devices were measured in a cryogenic probe system ($\sim 1 \times 10^{-6}$ Torr base pressure) with a Keithley 4200 semiconductor analyzer using a two probe Si back-gate configuration.

3. Results and discussion

MoS₂ flakes were transferred to highly doped Si/SiO₂ (150 nm) wafers by repeated mechanical cleavage from a bulk crystal using adhesive tape. Figure 1(a) shows an optical microscope (OM) image of several MoS₂ flakes having 1, 2, 4, 7, 10, and 15 layers. Note that layer number was determined with AFM measurements. From the line scan of AFM images shown in figures S1(a) and (b), the thicknesses of

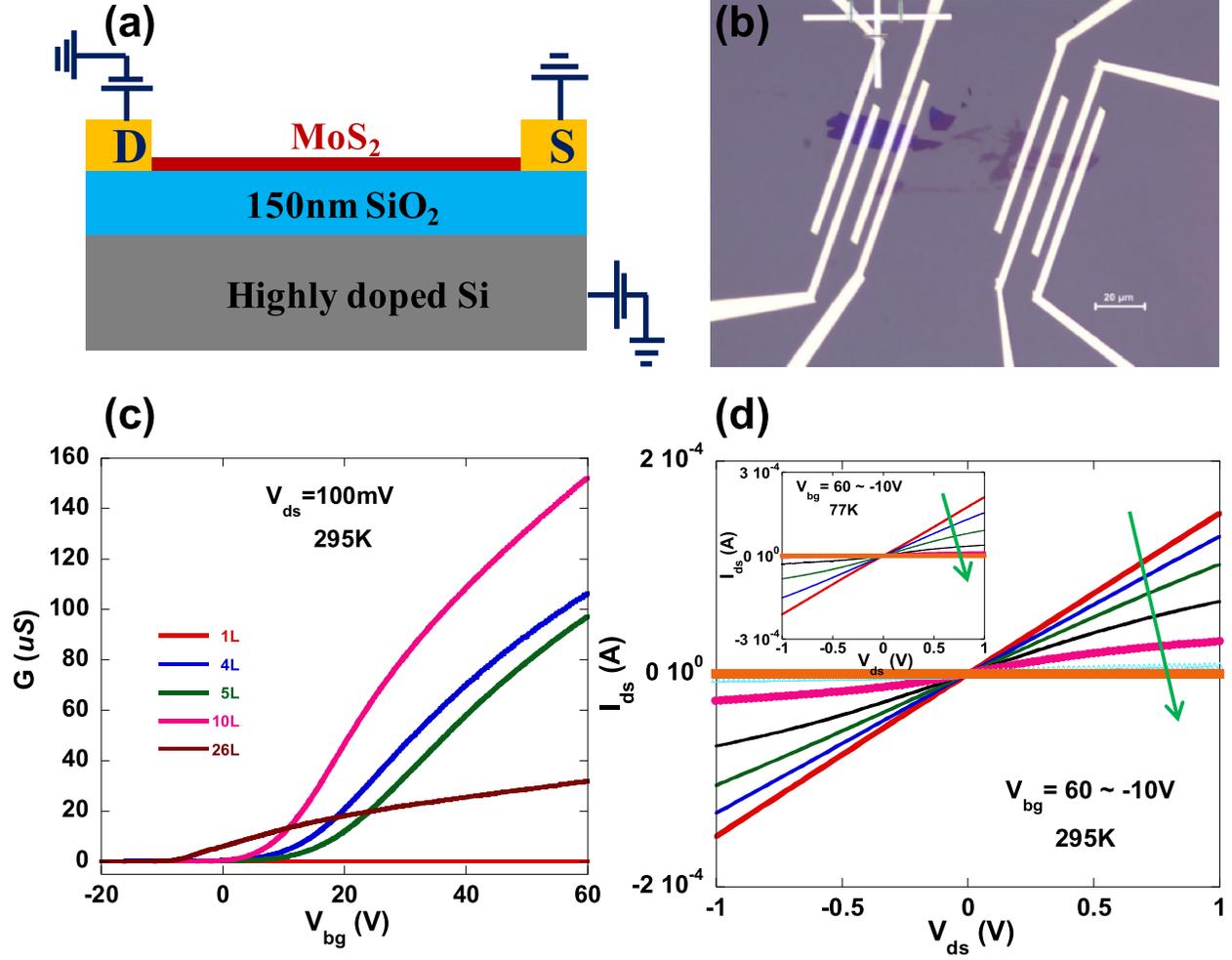


Figure 2. (a) Schematic of the MoS₂ FET devices that were fabricated on SiO₂/Si. (b) Optical microscopy image showing a plan view of the MoS₂ FET devices with electrodes. (c) Flake conductance versus back gate voltage at $V_{ds} = 100\text{ mV}$ showing n-type behavior in all cases. (d) The I_{ds} - V_{ds} curves for the 10 layer thick device demonstrating linear behavior for back gate voltage from -10 to 60 V , indicating ohmic contact both at room temperature and 77 K (inset).

flakes are 0.8 and 3 nm corresponding to mono and four layers, respectively. As shown in figure 1(b), Raman spectroscopy was performed to measure the characteristic peaks of MoS₂ associated with the E_{2g}^1 (in plane) and A_{1g} (out of plane) vibrational modes, and measure their shifts with thickness. The E_{2g}^1 peak showed a red shift with increasing thickness, suggesting stacking-induced structural changes or the dominance of a long range Coulomb interaction in few layers MoS₂ [33]. In contrast, the A_{1g} peak showed a blue shift with increasing thickness, owing to a higher force constant resulting from interlayer coupling [33, 34]. To ensure process uniformity, all the MoS₂ FETs were fabricated on a single wafer using standard electron beam lithography, yielding devices numbering in the tens with various thicknesses. Figure 2(a) shows a schematic of the MoS₂ FET devices and (b) shows an optical micrograph of a typical device in plan view.

The transport characteristics of the MoS₂ FET devices were measured from 295 K down to 77 K , and figure 2(c) is a

plot of conductance (G) as a function of back gate voltage (V_{bg}) for several thicknesses. Note that all the devices exhibited n-type behavior, and conductance was defined as $G = I_{ds}/V_{ds}$, where I_{ds} was the source-drain current, and V_{ds} was the source-drain voltage (taken as 100 mV for all cases). The I_{ds} - V_{ds} characteristics of a 10L ($\sim 7\text{ nm}$) device as a function of V_{bg} are shown in figure 2(d), while the inset indicates this linear behavior is maintained down to 77 K . Note that all the transport curves were measured at low bias $V_{ds} = 100\text{ mV}$ minimize the effect of contact resistance, which was negligible in the present work. The field effect mobility was extracted from the linear region of the device transfer characteristics using the equation $\mu = \left(\frac{L}{WC_{ox}}\right)\left(\frac{\Delta G}{\Delta V_{bg}}\right)$, where L was the channel length, W was the channel width, and $C_{ox} = 2.3 \times 10^{-8}\text{ F cm}^{-2}$ was the capacitance between the channel and the back gate per unit area, and taken as $C_{ox} = \epsilon_0\epsilon_r/d_{ox}$, where $\epsilon_0 = 8.85 \times 10^{-12}\text{ F m}^{-1}$, $\epsilon_r = 3.9$ and $d_{ox} = 150\text{ nm}$. A mobility as high as $70\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ was

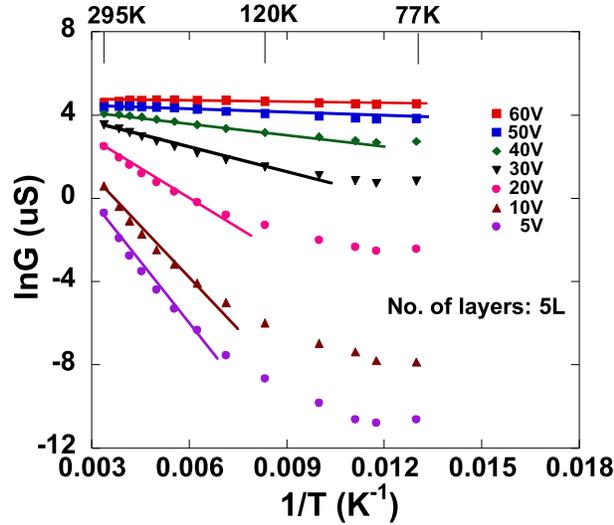


Figure 3. Arrhenius plot of conductance in a 5L device for back gate voltages ranging from 5 to 60 V. The solid lines are an aid to the eye, and show that for temperatures greater than ~ 120 K, the conductance is thermally activated, indicating charge transport is dominated by phonon limited scattering.

achieved at 295 K for a 5L device, which is in agreement with the value reported for few-layer devices using the same back gate geometry and two-probe measurement [35], and even higher than the $0.1\text{--}10\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ value reported for monolayer MoS₂ [7, 22]. This is mainly due to the higher density of states and lower Schottky barrier found in multi-layer MoS₂. Although other reports stated the higher mobility was obtained by utilizing top-gating or dual-gating configuration for mono- and few-layer MoS₂ devices [7, 24, 25, 36, 37], it was beyond the scope of our study. At 77 K, a mobility as high as $110\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ was achieved for a 5L device. Figure 3 is a plot of conductance as a function of temperature for various back gate voltages for a 5L device, and indicates that charge transport for few-layer MoS₂ is a thermally activated process at high temperature—i.e., Arrhenius in nature. Consequently, phonon limited scattering is the dominant transport mechanism at high temperatures. Note that the measurement was also carried out for different thicknesses (see figure S2 for 4L and 12L devices (stacks.iop.org/NANO/27/165203/mmedia)), and these too were found to be in agreement with a thermally activated model. Although some reports have shown the phonon scattering mechanism dominating in high and low temperatures [22, 37, 38], the weaker temperature dependence noted in our case below 100 K and at low back gate voltage was associated with low carrier density, and transport in this temperature regime was possibly attributed to a hopping mechanism through localized states [32].

In order to elucidate how mobility changed with MoS₂ thickness, it was plotted as a function of MoS₂ thickness (1L to 26L) for two temperatures as in figures 4(a) and (b). Similar trends in mobility were also found by Das *et al* [23] and Li *et al* [39] at room temperature, leading them to conclude Coulomb scattering from charged impurities and a

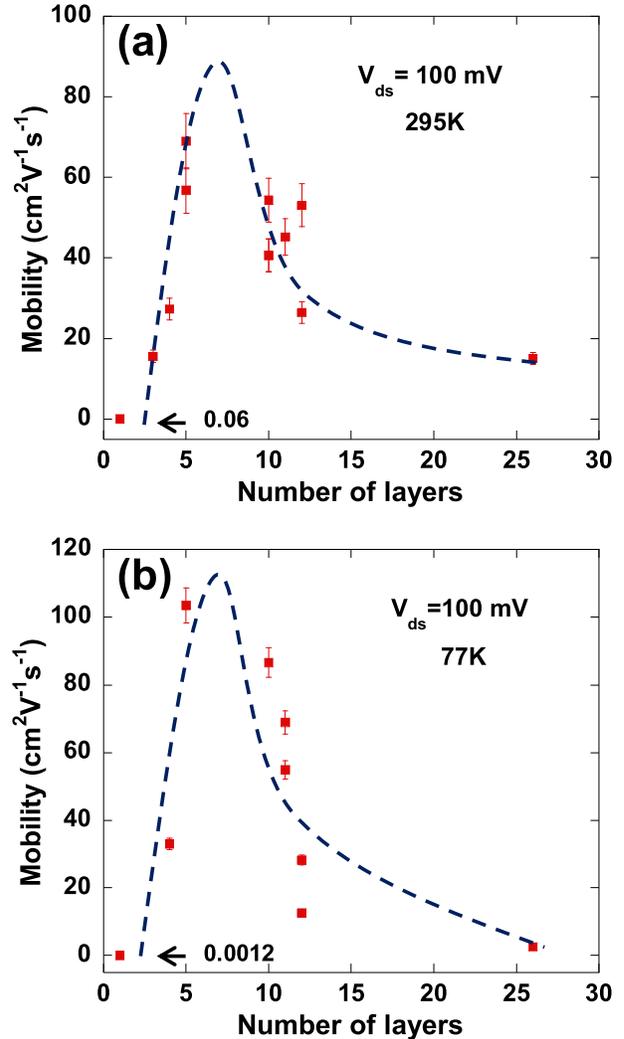


Figure 4. Mobility versus flake thickness for MoS₂ devices measured at 295 K (a) and 77 K (b), indicating an optimal thickness between 5L and 10L for maximum mobility in back-gated MoS₂ FET devices. The dashed blue line is a guide to the eye.

resistor network mechanism were responsible for the observed behavior. More specifically, as thickness increases, the effect of the substrate or charge impurities can be mitigated to some extent, leading to a mobility enhancement. However, the series resistance associated with an increasing number of interlayers [23, 40, 41] reverses this trend, and further increases in thickness reduces the mobility. At room temperature, our devices had a peak mobility of $60\text{--}70\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for a thickness of 5L–10L. At low temperature, this value increased to $110\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for a 5 layer device.

There are some reports [22, 25] indicating that the mobility of single- and few-layer MoS₂ devices peaks at 200 K and 160 K, respectively, but a systematic study of thickness dependence is not included. Although the charge transport with respect to different scattering mechanisms had been proposed, the surrounding dielectrics or reduced

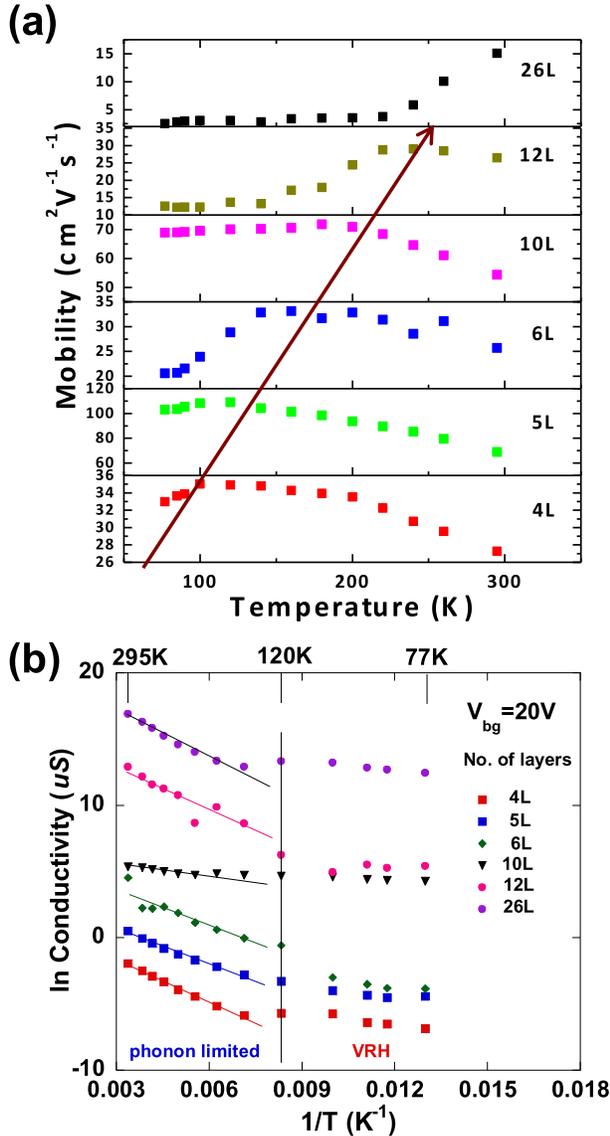


Figure 5. (a) Plot of mobility as a function of temperature for different device thicknesses, showing a transition in peak mobility temperature toward higher temperatures for increasing thickness. (b) Plot of conductivity versus temperature shows that phonon scattering dominates in high temperature regime (and low carrier density, $V_{\text{bg}} = 20\text{V}$), while variable range hopping dominates for lower temperatures, giving a much weaker temperature dependence.

Coulomb scattering from charge impurities were considered critical factors for improved mobility [42]. To shed more light on the subject, we thermally cycled 4L, 5L, 6L, 10L, 12L and 26L thick devices, and plotted their mobility as function of temperature as in figure 5(a). As the figure shows, we found that the temperature at which the mobility peaks, increased with thickness. From Raman, the E_{2g}^1 peak corresponding to an in-plane vibrational mode was observed to red shift for increasing thickness, while the A_{1g} peak associated with an out-of-plane vibrational mode was blue shifted. Since the mobility for higher temperatures was found to follow a

thermally activated process—i.e., it was dominated by phonon limited scattering related to lattice vibrations—we can possibly attribute the shift in peak mobility temperature with thickness to weaker electron–phonon interactions in thicker devices. Coulomb scattering due to charged impurities may also weaken electron–phonon interactions in thicker MoS_2 , again favoring a shift in the peak mobility temperature toward higher temperatures.

Kaasbjerg *et al* [43] have shown theoretically that the mobility due to optical and acoustic phonon scattering in monolayer MoS_2 increases with decreasing temperature, and follows the expression $\mu \sim T^{-\gamma}$, where the value of γ is dependent on the scattering mechanism. By fitting the data in figure 5(a) in the high temperature regime, values for γ were found to range from 0.5 to 0.7, and were smaller than the theoretical prediction of 1.69 for monolayer MoS_2 , indicating that homo phonon mode quenching may be active in thicker devices, as was suggested in recent complimentary work on monolayer MoS_2 in top-gating configuration [22] and bilayer MoS_2 [27]. In order to shed additional light on the dominant mechanism in our MoS_2 FET devices, conductivity as a function of temperature was plotted with thickness for carrier densities (n_{2D}) in the range of 5.8×10^{11} – $3.9 \times 10^{12} \text{cm}^{-2}$ at $V_{\text{bg}} = 20\text{V}$ as shown in figure 5(b). The carrier density is given by the expression $n_{2D} = C_{\text{ox}} \Delta V_{\text{bg}} / e$, where $C_{\text{ox}} = 2.3 \times 10^{-8} \text{F cm}^{-2}$ is the capacitance, $\Delta V_{\text{bg}} = V_{\text{bg}} - V_{\text{th}}$ (threshold), and $e = 1.6 \times 10^{-19} \text{C}$ is the elementary charge. In the high temperature regime ($T > 120\text{K}$), these curves follow a thermally activated process dominated by phonon limited scattering with a temperature dependence of $\sim T^{-1}$. Below 120 K, we attribute the weaker temperature dependence to variable range hopping (VRH) behavior due to low carrier densities or sulphur vacancies [32]. This hopping transport has been seen in graphene nanoribbons due to localized states at low temperatures [44].

Figure 6(a) shows the conductivity (e^2/h) of our 10L thick device as a function of back gate voltage (V_{bg}) and temperature. When gate voltages are below 40 V, the conductivity decreases with decreasing temperatures, indicating insulating behavior, whereas for gate voltages higher than 40 V, the temperature dependence is reversed, showing metallic behavior. The crossover from insulating to metallic conductivity is shown in more detail in figure 6(b). Note that this metal-insulation transition (MIT) behavior was only observed in our thinner devices (i.e., $< 10\text{L}$). For thicker ones, the conductivity always decreases with decreased temperature (insulator behavior) at all gate biases (see figure S3 for 5L and 26L thick devices), suggesting a threshold thickness for the transition. It is interesting to note that a screening length of 5 nm ($\sim 7\text{L}$) for unannealed MoS_2 FET devices has been reported, and was due to the trapping states induced by absorbed water molecules on the MoS_2 surface [45], analogous in our case to the possible production of a 2D electron gas with higher carrier density with less effect of localized states in devices thinner than 10 layers. With the encapsulation of high dielectric materials such as HfO_2 , the MIT behavior has been observed for monolayer MoS_2 devices due

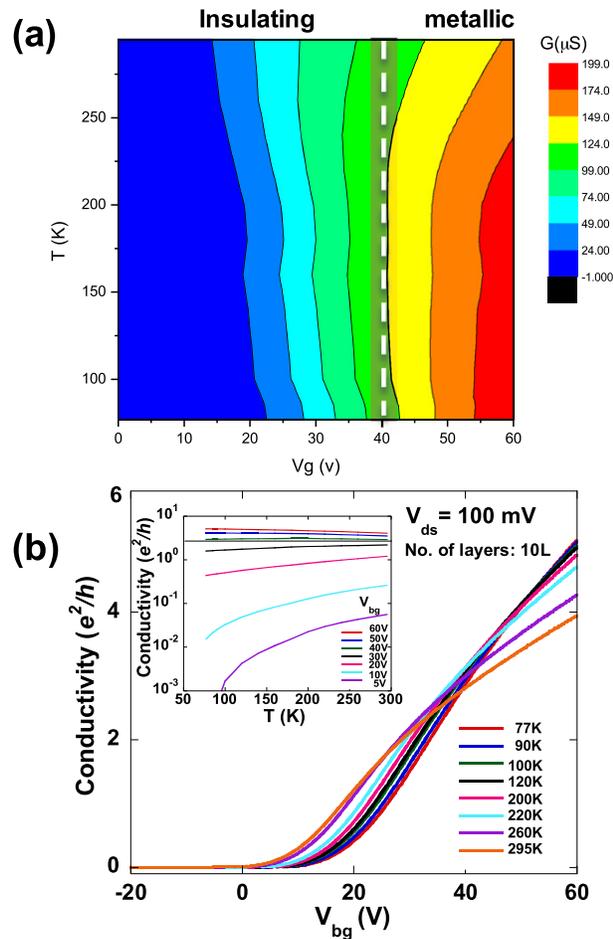


Figure 6. (a) Color plot of the conductivity as a function of temperature and gate voltage. (b) Conductivity as a function of gate voltage for different temperatures. The crossing around $V_{bg} \sim 40$ V indicates the change in temperature dependence. Inset shows the plot of temperature dependence of the two-terminal conductivity at different gate voltages from 5 to 60 V.

to impurities screening and high carrier densities [22]. In addition, the Ioffe–Regel criterion has been examined with the existence of a MIT for 2D semiconductors [46, 47]. According to the criterion, $k_F \cdot l_E \gg 1$ indicates a metallic phase, while $k_F \cdot l_E \ll 1$ indicates an insulating phase, where $k_F = (2\pi n_{2D})^{1/2}$ is the Fermi wave vector and $l_E = \hbar k_F \sigma / n_{2D} e^2$ is the mean free path of an electron. In our device, $k_F \cdot l_E = 2.84$ at the crossing point $V_{bg} = 40$ V (corresponding to a carrier density $n_{2D} = 4.7 \times 10^{12} \text{ cm}^{-2}$), which is in agreement with the theoretical prediction.

4. Conclusion

In conclusion, MoS₂ FET devices based on exfoliated mono- and few-layer crystals have been successfully fabricated, and conductance and mobility measurements have been made as a function of temperature. A mobility as high as $70 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was achieved in a 5 layer thick device.

Thickness-dependent mobility trends were observed at 295 K and 77 K, and provided an optimal thickness in the range of 5 layers to 10 layers for high performance applications. For each thickness, the mobility rises with increasing temperature to a peak. This peak mobility occurs at progressively increasing temperature with increasing thickness, which indicates that the Coulomb scattering due to charged impurities gradually dominates the charge transport in 2D MoS₂ crystals for thicker devices. Temperature-dependent conductivity measurements for different gate voltages reveal a metal-to-insulator transition for devices thinner than 10 layers. This study advances the understanding of fundamental charge transport mechanisms in few-layer MoS₂, and indicates the promise of few-layer transition metal dichalcogenides as candidates for potential optoelectronic applications.

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